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1 **Memory array architecture and decoding scheme for 3V only sector
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*Kobayashi, S.; Nakai, H.; Kunori, Y.; Nakayama, T.; Miyawaki, Y.; Terada, Y.; (
H.; Ajika, N.; Hatanaka, M.; Miyoshi, H.; Yoshihara, T.;*
VLSI Circuits, 1993. Digest of Technical Papers. 1993 Symposium on , May 19-
1993
Page(s): 97 -98

[Abstract]   [PDF Full-Text (384 KB)] **IEEE CNF**

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2 **Memory array architecture and decoding scheme for 3 V only sector
erasable DINOR flash memory**
*Kobayashi, S.; Nakai, H.; Kunori, Y.; Nakayama, T.; Miyawaki, Y.; Terada, Y.; (
H.; Ajika, N.; Hatanaka, M.; Miyoshi, H.; Yoshihara, T.;*
Solid-State Circuits, IEEE Journal of , Volume: 29 Issue: 4 , April 1994
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1 **A new decoding scheme and erase sequence for 5 V only sector eras;
flash memory**
*Nakayama, T.; Kobayashi, S.; Miyawaki, Y.; Futatsuya, T.; Terada, Y.; Ajika, N
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[Abstract]   [PDF Full-Text (164 KB)] **IEEE CNF**

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H.; Ajika, N.; Hatanaka, M.; Miyoshi, H.; Yoshihara, T.;*
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[Abstract]   [PDF Full-Text (384 KB)] **IEEE CNF**

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3 **Memory array architecture and decoding scheme for 3 V only sector
erasable DINOR flash memory**
*Kobayashi, S.; Nakai, H.; Kunori, Y.; Nakayama, T.; Miyawaki, Y.; Terada, Y.; (
H.; Ajika, N.; Hatanaka, M.; Miyoshi, H.; Yoshihara, T.;*
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8 **A 5-V-only 16-Mb flash memory with sector erase mode**
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